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/Kathryn Marley/
Kathryn Marley

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of inventor(s):
Lukas P.P.P. van Ginneken et al.

Application No. **10/828,547**

Confirmation No. **3884**

Filing Date: **19 April 2004**

Title: **Timing Closure Methodology Including Placement with Initial Delay Values**

Group Art Unit: **2825**
Examiner: **Vuthe Siek**

CUSTOMER NO. 36454

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF MARTIN WALKER

I, Martin G. Walker, Ph.D., provide the following declaration:

1. I have been retained as an expert consultant by Synopsys. This declaration is based on my personal knowledge and experience as well as my investigation in this matter and reflects my expert opinions on certain issues to which I may testify.

I. EDUCATION AND EXPERIENCE.

2. My CV (Exhibit A) contains an overview of my thirty years of experience in the field of Electronic Design Automation ("EDA") software systems. I received a BSEE from the Massachusetts Institute of Technology in 1973, and MSEE from Stanford University in 1976, and a PhD. in electrical engineering from Stanford University in 1979. My work experience includes direct work with EDA software, both as a developer and as a user.

3. From 1983 to 1989, I was the founder and Chief Technical Officer at Analog Design Tools, Inc. In my work at Analog, I was a founder and founding CEO. I was primarily responsible for writing the original business plan and raising the venture capital necessary to launch the company and recruiting the staff. Later, I was responsible for all technical aspects of

product definition and development. My efforts were instrumental in growing Analog from a start-up company to a leader in the field of analog design automation.

4. From 1990 to 1994, I was a founder and Executive Vice President of Symmetry Design System ("Symmetry"), which specialized in product design and consulting for the electronic design marketplace. In this role, I was instrumental in development of Symmetry's products.

5. In 1995, I founded a company called Frequency Technology (now Sequence Design) ("Sequence") that develops EDA software for the design of advance system-on-a-chip integrated circuits. Sequence's products have become the de facto industry standard for parasitic extraction, circuit optimization and RTL power analysis. As Chief Executive Office, director, and Chief Scientist at Sequence, I was involved in overseeing the development of the company's products and technologies. I also took an active role in recruiting the technical and business staff.

6. I am named as an inventor in three patents in the field of electronic design automation.

II. PUBLICATIONS AND SEMINARS.

7. I have published over fifty articles relating to EDA software, including technical papers in peer-reviewed journals and an invited article in the International Electronic and Electrical Engineers (IEEE) Spectrum, and I have presented papers in various conference proceedings. I have authored numerous opinion pieces published in journals, such as EE Times, that served to establish and promote EDA technology and tools. I have also organized many seminars, to educate others about the emerging innovative concepts in the EDA industry.

8. In addition to my professional associations, I am an inventor of three issued United States Patents. Additionally, I have published over 50 papers, abstracts, and articles. My publications during the last ten years are as follows:

- Martin G. Walker, *Modeling the wiring of deep submicron ICs*, IEEE Spectrum v37n3, March 01, 2000 at pp. 65-71
- Dr. Martin G. Walker, Dr. Keh-Jeng (KJ) Chang, Dr. Christopher J. Bianchi, *SIPP's Why Do We Need a New Standard for Interconnect Process Parameters?* VLSI: Systems on a Chip, Kluwer Academic Publishers, December, 1999

- Martin Walker, *Timing Errors Haunt Interconnects*, Electronic Engineering Times n1021, August 17, 1998
- Martin Walker, *Interconnect Analysis Must Move to 3-D*, Electronic Engineering Times n980, November 10, 1997
- Martin G. Walker, *The Guardband Crisis*, Electronic Engineering Times n929 November 25, 1996 at p. 43

In addition to the foregoing, I also submitted opinion pieces to Integrated Systems Design (May 1997), Electronic Business (April 1998), and EE Times (June, July, and September 1998).

III. AWARDS AND RECOGNITIONS.

9. Under my leadership as Chief Executive Officer, in 1999, Frequency Technology was given the recognition of "Cool Company" by Fortune Magazine.

10. My innovative contributions to the Analog Workbench won Analog the 1984 Electronic Products New Product of the Year award.

11. In 1976, in recognition of my contributions to the design of GaAsFET amplifiers, I was awarded the IEEE Microwave Applications award.

12. For my inventions and innovations in the EDA industry, I have been awarded three patents by the United States Patent and Trademark Office.

IV. BACKGROUND.

13. Prior to the mid 1990's, the design of ICs could be conveniently broken down into two distinct phases, electrical design, and physical design as shown in Figure 1. Electrical design refers to the process of determining the functionality of the IC. As shown in Figure 1, the specific cells and how they would be interconnected are defined during this phase with reliance on specialized EDA tools. The performance of the IC could also be accurately determined during this phase. Performance is determined using a specialized tool called "timing analysis." Timing analysis as was known in this time period required that the cells (particularly the drive strength and input capacitance) were specified prior to analysis[1]. In particular there were no

[1] Timing analysis relied on a sub-tool called a "delay calculator." The delay calculator combined the drive strength of one stage with the total load capacitance of the next stage to predict the

known tools that could determine the timing of a design without knowing the performance of the cells, which is in large part determined by the size of the cells. After assuring that their timing performance goals were met, IC designers could simply complete the electrical design and "hand it off" to another group to perform the physical design. This "handoff" included a netlist that identified the specific cells (including function and size) that would be used in the design of the integrated circuit. As shown in Figure 1, the handoff also included the timing information for the design.

14. The physical design group would use appropriate EDA tools (called "Place and Route") for determining the location of the cells on the IC as well as the wires used to interconnect the cells. For the most part there was little if any interaction between these groups. Importantly, the physical design group could pretty much complete the design of any electrical design handed to them. The electrical design group could pretty much be assured that their design would meet performance goals as well. Thus the design process was mostly straight-forward: electrical design followed by physical design, with little back and forth between these processes.

15. Performance of a design is determined by the performance of the cells (which are determined during the electrical design phase) and performance of the wires (which are determined only during the physical design phase). As long as the performance of the wires could be safely neglected compared to the performance of the cells, then the design flow would work smoothly.

16. However, by the early 1990s this design flow began to breakdown. As process technology continued to advance, the performance of the wires began to determine the performance of the IC. Worse, the performance of the wires could not be determined until the wires were designed during the physical design step. Thus the performance of the design would change after the design was placed. This necessitated that the electrical design must be optimized again after placement. But this optimization changed the size of the placed cells, necessitating a new placement, which required new optimization, which resulted in new cells, which must be placed again.

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delay. Since drive strength and load capacitance go hand-in-hand with cell size, the requirement that drive strength and cell size are known necessarily implies that the size of the cells are known.

17. Thus the electrical design team could no longer be assured that their design would meet specifications until more detailed physical design was completed. Even worse for the IC companies, the formerly linear process of IC design was now an iterative process, and no one could predict when or if a design would be complete and ready to release to production. Thus, for example, the next new game console, promised for Christmas, might not reach the stores until March of the following year.

18. In the early 1990s, tools were developed using a first attempt to address this problem. The design flow represented by these tools, often called "timing driven placement," is shown schematically in Figure 2. As can be seen, this design flow required considerable more timing analysis, thus the performance of timing analysis at all stages of the design flow became critical. Importantly, however, this flow followed the same path as the original flow in that the specific cells (and therefore size of cells specified) during electrical design and the netlist representing the design (and inherently including the size of the cells) was created during the electrical design phase.

19. This flow is discussed in more detail in the background section of this application as filed (hereinafter the "Present Application"). Figure 3 is a somewhat more detailed view of the design flow and begins with the last steps of the synthesis program, and shows the explicit steps of determining the timing of the design. As can be seen, the cells are first selected during the electrical design phase. Then these cells are later optimized during the physical design phase.

20. However, by the mid 1990s even this approach began to break down since the physical tools could no longer meet the performance goals specified at signoff. Thus the physical group would hand the design back to the electrical design group to perform a redesign. The electrical group would create a new design that the physical group would try to complete. But this iterative process might require considerable time to complete. Thus the design process itself was in jeopardy of failing. Thus, in order to restore order to this process, a new generation of EDA tools that allow electrical design and physical design to proceed simultaneously would be required. This fundamentally new design flow is the subject of the invention in the patent at issue. In Figure 4, the elements of pending claim 2 are shown in the context of this new design flow.

21. Figure 4 is fundamentally distinguished from Figure 3 by two steps. First, the performance of the design is determined prior to selecting the specific cells. Thus the timing

analysis is performed *before* specific cells are selected, and thus the cells have an undetermined size. Although the details of this sizeless timing analysis are not part of pending claim 2, the specification as filed teaches that the assigning delays to cells can be accomplished prior to specifying the size or area of the cells. See for example pp 33-35. This method of determining timing was not known in the art, and, at the effective filing date of the Present Application, there were no available EDA tools that utilized this method to determine timing.

22. Second, because performance could be determined before cell sizing, the step of selecting cell sizes could be postponed until after the location of the cells were determined. Since the size of the cells was determined after the position was known, the problem of the endless placement/optimize loop was solved.

23. During the electrical optimization process, the new design flow is shown schematically in Figure 4. Figure 4 shows that the sizes of the cells are not determined until after the location of the cells has been determined. Thus the infinite loop described above is replaced again by a linear design flow.

V. DETAILED ANALYSIS OF CLAIM 2 vis a vis the Tsay reference.

24. Claim 2 recites as follows:

2. An automated method for designing an integrated circuit layout with a computer, comprising:
(a) selecting a plurality of cells that are intended to be used in the integrated circuit layout;
(b) determining initial delay values associated with the cells prior to determining an initial placement of the cells; and
(c) performing an initial placement of the cells, including determining an initial size or area of the cells in response to the initial placement.

25. As outlined above, the Tsay reference does not teach either of two fundamental aspects of claim two: timing before sizing, and placement before sizing.

26. Timing analysis must be used to associate delays with cells. Based on my experience in the EDA industry, I know that at the time of the filing of the Tsay reference, the all methods to perform timing analysis required that the sizes of the cells be specified. There is no discussion of performing timing analysis of unsized cells as in the Present Application. Thus timing of a design prior to determining the cell sizes is certainly not enabled in the Tsay reference.

27. Further, the input to the method described in the Tsay reference is a netlist, preferable in EDIF format. An EDIF netlist necessarily specifies the cells used in the design, including the size of the cells. Thus the Tsay method receives a design in which the cells are

already specified. Then, following the flow outlined in Figure 3, these cells are optimized based on placement. However, there is nothing in the Tsay reference which teaches that the cells are placed before the sizes are provided.

VI. Discussion of Examiners Comments re the Tsay Reference.

28. The examiner states that the Tsay reference teaches that the initial size or area of cells are determined in response to the initial placement (see ¶ 6 of the office action). However, a close reading of the Tsay patent discloses that the input to the system described in Figure 3 is preferable an EDIF netlist. See 3:42-46 "a user imports … a list of the wiring interconnections between devices with one of the EDIF files." An EDIF file necessarily references specific cells from a cell library that have specified size or area. Next, the Tsay reference teaches that the system described in Figure 3 (in particular blocks 112, 124, and 128) determine the initial placement of the cells. Thus the initial size is determined before prior to the operations discussed in the Tsay reference. Since the cells had a pre-determined size at the time the Tsay system computed their placement, the Tsay reference does not (and cannot as a matter of logic) teach how to perform an initial placement prior to determining the size or area of the cells.

29. Similarly, step (b) of Claim 2 recites "determining initial delay values associated with the cells prior to determining an initial placement of the cells." Since this step must occur prior to step (c) " … determining an initial size or area of the cells," it follows that the initial delay values must be determined prior to determining the size of the cells. The examiner states that the system in Figure 3 provides such a determination. However, for the reasons stated in the previous paragraph, the input to the Tsay system receives as input cells with sizes or areas already specified. If follows that the Tsay reference does not teach how to determine initial delay values prior to determining an initial placement of the cells.

30. In contrast, the Present Application does teach how to make such determination. In particular, the specification describes in detail the use of the theory of logical effort to assign delay values to cells prior to determining the size. In contrast to the timing analysis systems generally known at the time of the Tsay reference, logical effort is used to associate a "gain value" to each cell. Gain is defined as the ratio of total output capacitance to input capacitance. (Input capacitance is directly related to the size or area of the cell.) Thus gain only defines a capacitance ratio but doesn't specify the size or area of the cell. The theory of logical effort

teaches that this gain value determines delay. Thus by specifying the gain of the cell, the delay is uniquely determined without specifying the area of the cell.

31. It is my belief that the examiner may not have appreciated this fundamental aspect of the instant invention, and assumed that traditional timing analysis was used to determine the initial delay values. I believe that the examiner may have then assumed that since traditional timing analysis required that the size or area of the cells be specified, that step (b) was performed using cells specified from a cell library, which contained a specified initial size or area of the cells.

32. My belief is engendered by the examiner's "Remarks" (¶ 20). For instance, the examiner states that "When sizing a cell, the cell (i.e. a buffer for example) size must be know before hand." Although this statement correctly reflects prior art systems, it does not reflect the present invention. Indeed Claim 2 states in part "determining an *initial* size or area of the cells in response to the initial placement." (emphasis added) Thus the plain language of the claim (that the initial size is determined *after* placement) contradicts the examiner's summary.

33. The examiner goes on to state that "a designer does not know what to do if a cell size is not know[n]." I presume the designer is referring to design processes such as timing analysis and cell placement. Again, this statement properly reflects the prior art systems such as that discussed in the Tsay reference. However, the present invention does not have such requirements. For instance the claim 2 states in part "determining initial delay values associated with the cells prior to determining an initial placement" and prior to determining an initial size or area. As discussed above, timing analysis prior to specifying cell area was not generally known at the time of the invention, but the Present Application enables such analysis as discussed above.

34. Finally, the examiner states that "more buffers would provide more drivability capability to reduce delay to meet design requirement. Nothing is novel that concept." This statement is simply wrong. The Present Application teaches that adding buffers actually increases delay, but may reduce area. See pages 45-48. Again, the examiner's misunderstanding results from the lack of appreciation of the novel nature of the invention.

35. In summary, the novel invention described in the Present Application that enables timing and placement prior to determining the size or area of the cells clearly distinguishes the present invention from the Tsay reference. Further, it is clear that the examiner did not appreciate these fundamental differences.

VII. Other questions regarding the specification.

36. The examiner states in part that Figure 5 of the Tsay reference also discloses net weight calculations. A close reading of the Present Application however indicates that the net weight calculation is performed on cells whose sizes have not yet been determined. In fact, the net weight calculation is used to help determine the size of the cells. In particular, the net weight calculation is made using the "gain" of the cell (h_{ij} in equation 3). The concept of gain is entirely absent in the Tsay reference. Thus by logic, the Tsay reference cannot disclose the net weight calculation since it doesn't disclose one of the predicates for the calculation.

37. Finally, the examiner points to the discussion at 2:42-46 of the Tsay reference as evidence that the Tsay reference teaches timing optimization, sizing and logic synthesis. However, Tsay merely teaches that the method of timing analysis disclosed in the Tsay reference can be used as part of the prior art design flow, which requires that the size of gates be determined before timing and post-placement sizing optimization, and logic synthesis. For example, the Present Application contains a detailed discussion of important features of logic synthesis including structure optimizations and mapping before size of the cells are determined. There is nothing in the Tsay reference that remotely addresses such issues.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, §1001 and that such willful false statements may jeopardize the validity of any patent issuing from the above-identified Application, and related cases.

Martin Walker

14 June 2009
Date

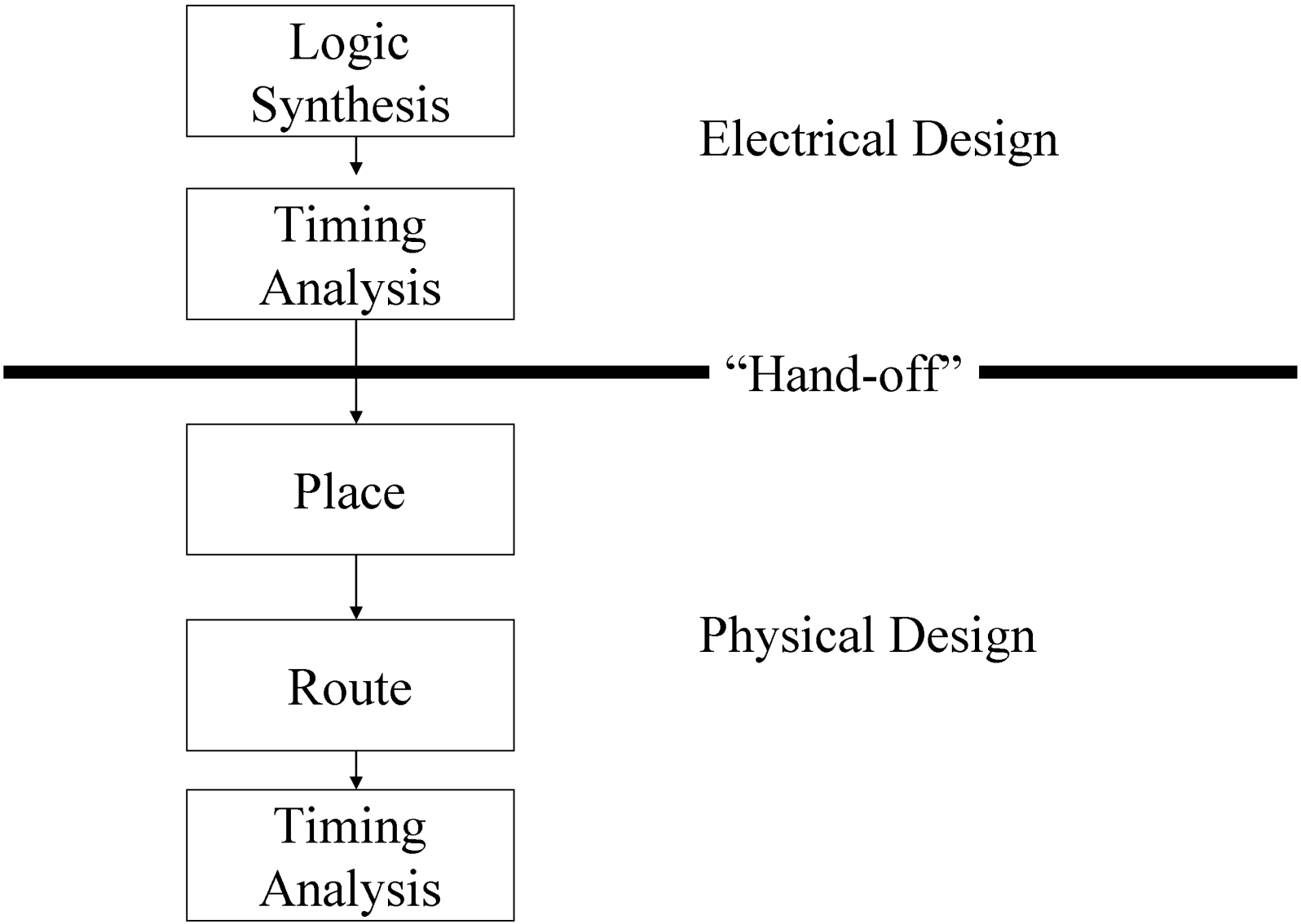

Figure 1. Traditional Design Flow

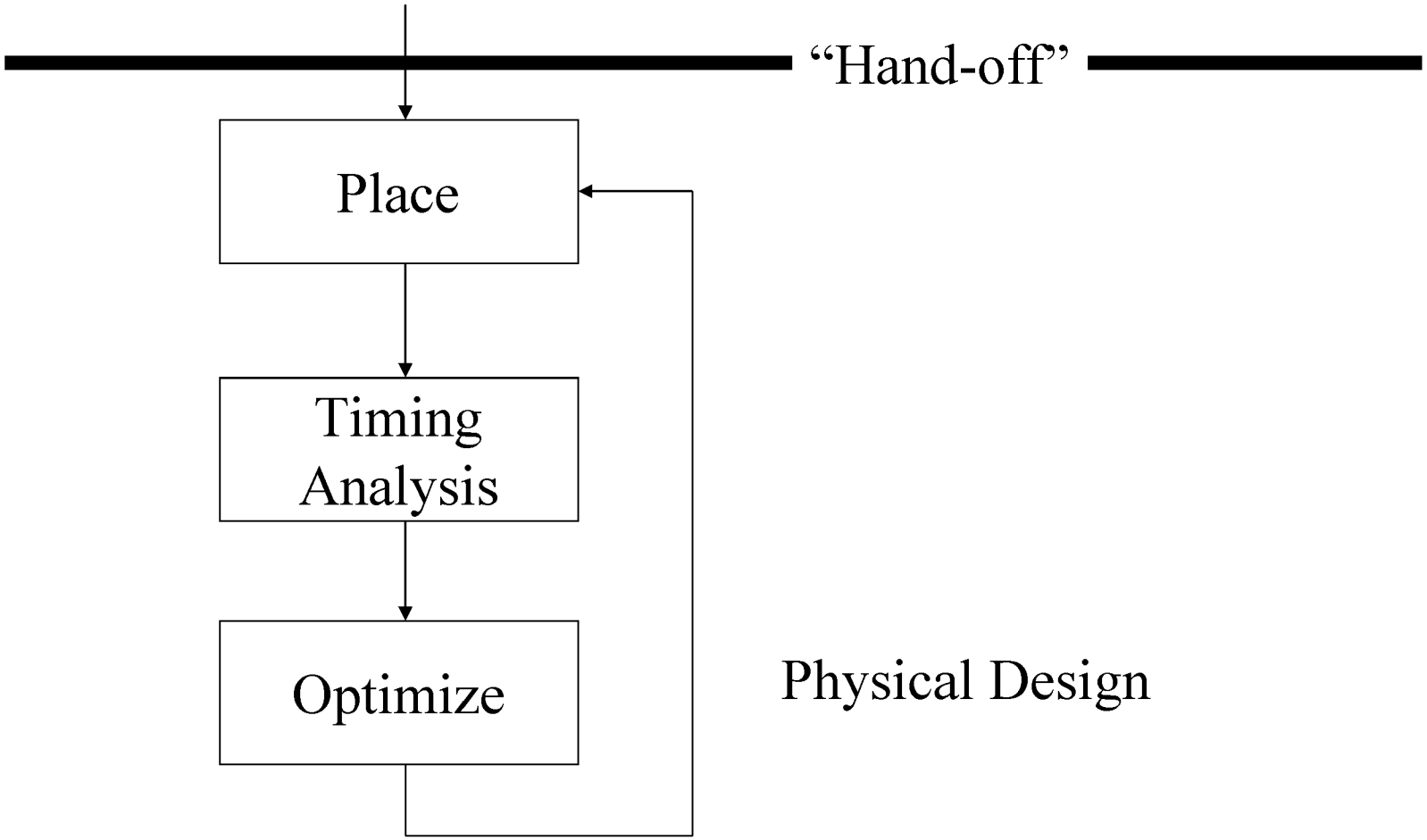

Figure 2. Timing-Driven Placement

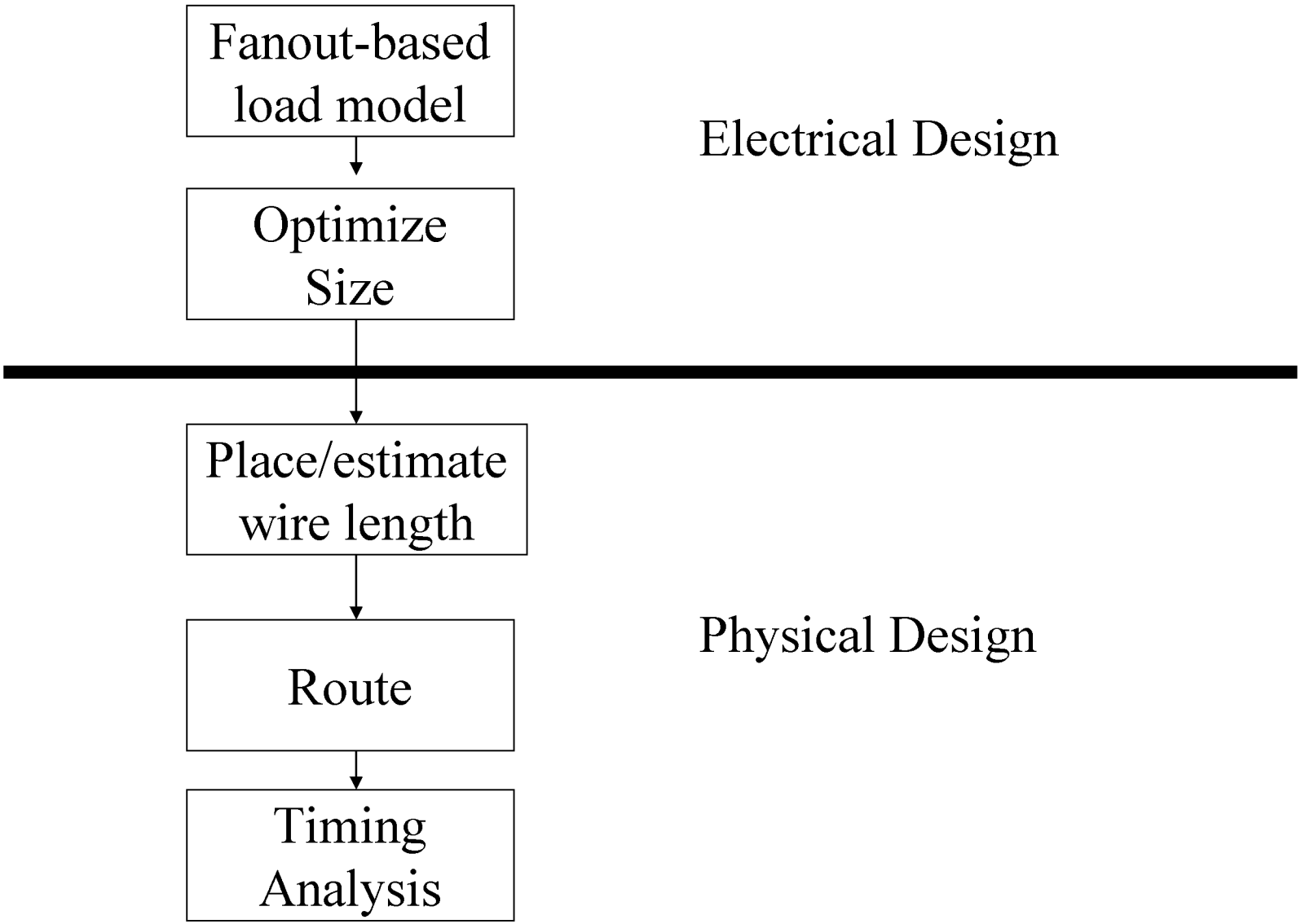

Figure 3. Details of timing-driven flow

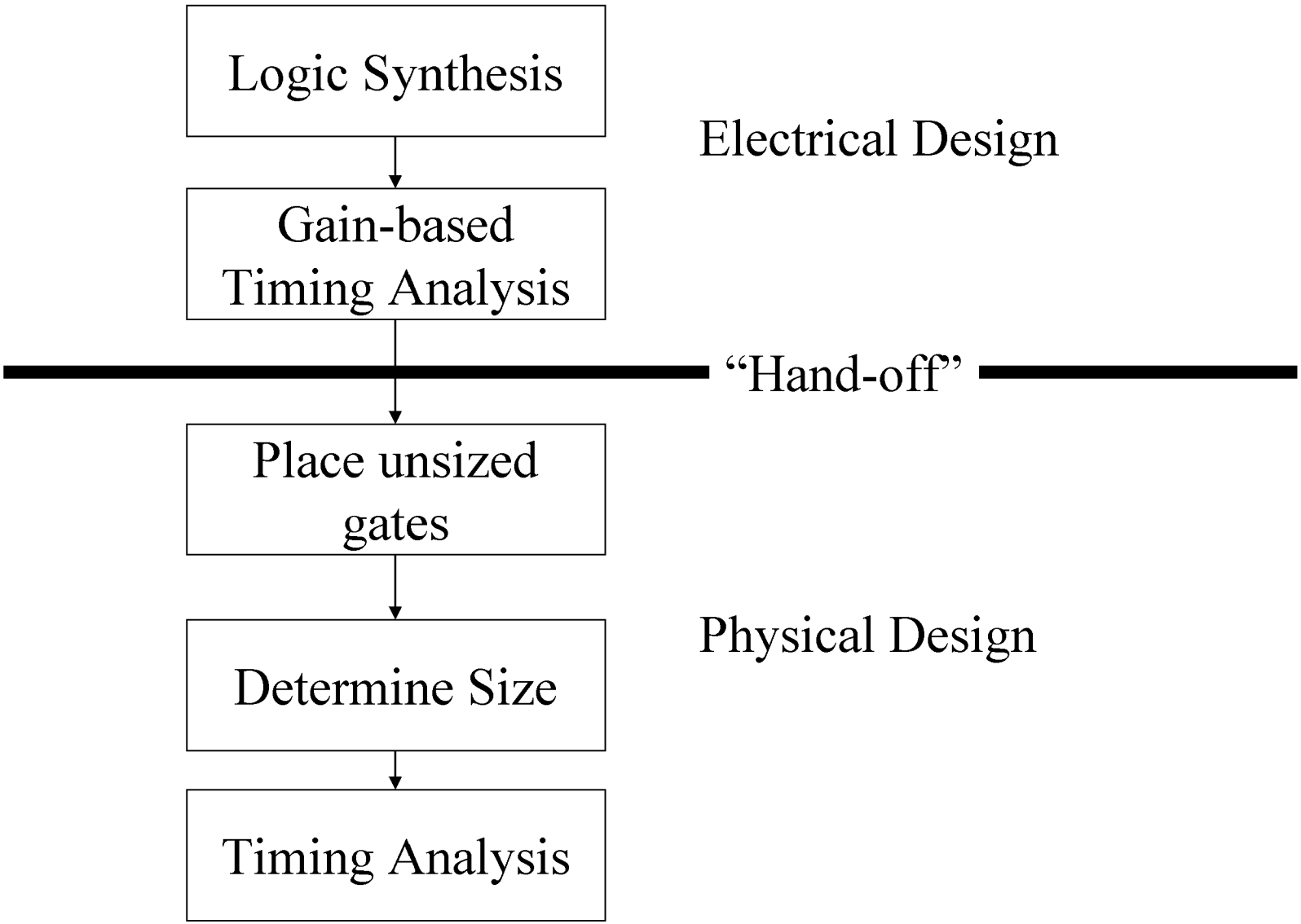

Figure 4. Constant delay flow

EXHIBIT A

Martin G. Walker, PhD
Consultant Curriculum Vitae

Expertise

IC Design
- EDA Software
- Digital circuit design and simulation
- Analog IC design and analysis
- Analog circuit design
- RF and microwave circuit design

Source Code
- Identification of copied source code
- Analysis of copied source code
- Analysis of alleged trade secret misappropriation
- Patent infringement of source code
- Copyright infringement of source code, including database schemas

Litigation Experience

Dr. Walker has testified in jury trials and arbitration involving software technology issues. He has been engaged as a "technology neutral" to assist in the resolution and adjudication of electronic discovery issues. Dr. Walker also has significant experience in giving deposition testimony and in preparing declarations and expert reports. Dr. Walker regularly works with attorneys to help articulate and manage the many technology issues that arise in complex litigation. He is particularly adept at explaining complex technology issues to lay audiences and, as such, has often been asked to present Markman tutorials and prepare demonstratives.

Industry Experience

Dr. Walker is a recognized expert with over 35-years of experience in design of integrated circuits, including analog, digital and RF/microwave circuits. His analog IC circuit design experience includes analog components such as PLLs, voltage regulators and linear systems. In the digital IC design Dr. Walker has experience at the circuit level, including such structures as ESD components, level shifters, sense amps, SDRAM circuits such as DDR sequencing circuits and On-Die Termination (ODT). His RF/Microwave design experience includes microwave components (such as amplifiers, oscillators, mixers and switches) as well as sub-systems (tuners, low-noise down converters, etc).

Dr. Walker has over 25 years experience in electronic design automation (EDA) software systems, simulation and circuit design and modeling. He is a recognized expert in the field of EDA systems, simulation, and modeling. He also has experience with the design of digital and analog IC, with verilog and VHDL analysis, synthesis of digital ICs such as flash memory controllers, analyses and verification of metal interconnects and related process technology.

He also has acquired expertise in the analysis of alleged source code copying. He has developed specialized analysis tools that help find the "needle" of copied code in the "haystack" of large source-code databases. He has identified existence of misappropriated code as well as helped to demonstrate the lack of evidence of misappropriation. During the course of his practice, Dr. Walker has analyzed such diverse code as EDA software, VoIP software, database schema, mail-list processing software, and stock-brokerage software. He is familiar with a wide variety of source-code repositories including CVS, RCS, Subversion, and Rational ClearCase.

Martin G. Walker, PhD
Consultant Curriculum Vitae

Litigation Projects

Date:	2000-02	**Thelen Reid (for Plaintiff)**
	Case:	Sequence Design vs various defendants
	Project:	Patent infringement relating to EDA software. Provided support for claim construction and infringement analyses.
	Status:	Settled
Date:	2001-03	**Dechert, LLP (for Plaintiff)**
	Case:	Silvaco v CSI
	Project:	Misappropriation of trade secrets, including copied source code. Analysis of source code written in the C language. Created the 2019(d) statement that described Silvaco's trade secretes and provided numerous declarations that supported this description. Testified at deposition regarding source code copying, other trade secret misappropriation, and business practices.
	Status:	Settled on terms favorable to plaintiff
	Testimony:	Deposition
Date:	2001-02	**FTI Teklicon (for IRS)**
	Case:	IRS vs taxpayer
	Project:	Analysis of valuation for tax purposes of EDA software and associated royalty streams.
	Status:	Completed
Date:	2001-02	**Dechert LLP (for Plaintiff)**
	Case:	Synopsys vs Nassda (patent infringement)
	Project:	Retained as testifying expert. Project involved analysis of electronic circuit simulation software written in the C programming language. Declaration, expert report, and deposition in support of claim construction. Declaration in opposition to Summary Judgment motion for non-infringement which was denied by the Court. Infringement analysis and expert report. Opposition to invalidity claims.
	Status:	Settled on terms favorable to plaintiff
	Testimony:	Deposition
	Expert Report:	Claim construction issues

Martin G. Walker, PhD
Consultant Curriculum Vitae

Date:	2001-04	**Dechert, LLP (for Plaintiff)**
	Case	Synopsys vs Nassda (State Action)
	Project:	Identification of misappropriated trade secrets relating to circuit simulation. Analysis of source code creation rates. Analysis of electronic evidence tampering. Assist with discovery issues. Manage electronic discovery of more than 300Gbytes of documents. Analysis and declarations regarding disk wiping and other evidence tampering by defendants led to the defendants' decision to settle on terms widely seen as extraordinarily favorable to Plaintiff
	Status:	Settled on terms favorable to plaintiff
Date:	2001	**Law offices of Al Reynaldo (for cross-defendant Aprés)**
	Case	Aprés vs Ho
	Project:	Misappropriation of EDA-related trade secrets
	Status:	Settled
	Testimony	Testified at jury trial regarding software algorithms and development process
Date:	2003-04	**Dechert LLP (for Plaintiff)**
	Case	Synopsys vs Nassda (patent infringement – '998)
	Project:	Claim construction analysis and declaration. There were 11 disputed terms. The Court adopted Dr. Walker's construction on all 11 terms, rejecting all of the defendants arguments.
	Status:	Settled pending FTC approval
Date:	2003-04	**Dechert LLP (for Respondent)**
	Case	CSI vs Silvaco
	Project:	Arbitration resulting from alleged violation of the terms of the settlement agreement.
	Status:	Arbitration completed
	Testimony:	Three-judge arbitration panel regarding CSI's licensing, support and maintenance of certain Silvaco trade secrets
Date:	2003-04	**Dechert LLP (for Plaintiff)**
	Case	HCL vs eKomas
	Project:	Analysis and identification of directly copied source code written in a web-host scripting language. The product at issue is a web-based application for loan management.
	Status:	Settled

Martin G. Walker, PhD
Consultant Curriculum Vitae

Date:	2004	**McDermott (for Defendant)**
	Case	Tera Systems vs InTime Software
	Project:	Patent infringement related to EDA software. Researched invalidity and supported claim construction.
	Status:	Settled
Date:	2004-05	**Dechert LLP (for Plaintiff)**
	Case	Silvaco vs CSI – OSC re Contemp
	Project:	Analysis and declaration regarding the Defendants' continued use of Silvaco trade secrets.
	Status:	Completed
	Testimony:	Bench trail
Date:	2004-05	**Dechert LLP (for Defendant)**
	Case	Siliconix vs AATI
	Project:	Patent infringement regarding method for manufacturing a semiconductor device. Support for claim construction and invalidity analysis. Researched prior art.
	Status:	Settled
Date:	2005	**Kirkland & Ellis LLP (for Defendant)**
	Case	Berry vs Fleming, et al.
	Project:	Source code copyright and misappropriation of trade secrets of an SQL database schema as well as associated source code. Reviewed source code at issue.
	Expert Report	Relating to software development, non-infringement of copyright, and analysis of forensic data to refute claims of electonic evidence spoliation
	Status:	Summary judgment of non-infringement of copyright for more than 90% of potential damages. Jury verdict awarding minimal damages for balance of claims
Date:	2005	**Dechert LLP and Wilson Sonsini (for Plaintiff and Cross Defendant Synopsys)**
	Case	Synopsys vs Magma (
	Project:	This matter involved theft of IP relating to EDA software as well as patent infringement in two venues. Analyzed Magma software written mostly in C++ for infringement identified historical software supporting invalidity of Magma patents. Provided support for claim construction and invalidity analysis.
	Status:	Settled on terms favorable to Synopsys.

Martin G. Walker, PhD
Consultant Curriculum Vitae

Date:	2005	**Browne & Woods LLP (for Defendant)**
	Case	Keywords vs ISE
	Project:	Investigated allegations of source code copying and copyright infringement of source code written in an interpreted language similar to perl. Declaration ISO of opposition to preliminary injunction.
	Status:	Settled
	Expert Report:	Regarding source code copying and inadequate description of alleged trade secrets

Date:	2005-06	**Jones, Day (for Plaintiff)**
	Case	Experian v. I-Centrix
	Project:	Investigating allegations of source code copying and misappropriation of trade secrets. The code was originally written in fortran, but then translated into the C programming language. Performed analysis of electronic data that suggested evidence tampering on the part of defendants.
	Status:	Settled
	Testimony:	Deposition
	Expert Report:	Identification of literal copying of source code as well as copied algorithms. The expert report identified methods the defendants used in an attempt to disguise the misappropriated code and algorithms.

Date:	2005	**Dechert LLP (for Plaintiff)**
	Case	Silvaco vs CSI End Users
	Project:	Analysis and declarations regarding the Defendants' continued use of Silvaco trade secrets.
	Status:	Stayed
	Testimony:	Deposition

Date:	2006	**Gordon Rees (for Defendant)**
	Case	FIS v. CalAmp
	Project:	Investigation of alleged misappropriation of trade secrets. Performed investigation and created expert report regarding the alleged misappropriation.
	Status:	Settled
	Expert Report:	Relating to alleged misappropriation of software trade secrets.

Date:	2006	**Gordon Reese (for Plaintiff)**
	Case	LiveOps v. Teleo
	Project:	Misappropriation of trade secrets, copyright infringement of VoIP software systems. Investigation to detect software copying.
	Status:	Settled

Date:	2005	**Dewey Ballantine (for Plaintiff)**
	Case	Matsushita v. MediaTek
	Project:	Patent infringement investigations (invalidity, claim construction, infringement) relating to various patents, including design techniques and DFM technology. Provided expert report regarding infringement and validity of the patents at issue.
	Status:	Settled
	Testimony:	Markman tutorial, for three patents at issue; deposition
	Expert Report:	Relating to infringement and validity of DFM patent related to processing of metallization structures.

Date:	2006	**Court-Appointed Technology Neutral**
	Case	Apple Resellers et al v. Apple Computer
	Project:	Technology neutral appointed by Judge Jacobs May in Superior Court of Santa Clara to resolve the parties disputes regarding proper production of electronic documents
	Status:	Settled
	Testimony:	Two hearings before the Court relating to several discovery motions
	Expert Report:	Explained technology and issues relating to the electronic production by the various parties.

Date:	2006	**Paul Hastings (for Defendants)**
	Case	iSmart International v I-Docsecure
	Project:	Plaintiffs allege that Defendants misrepresented certain technology in the context of an equity investment. Investigated to determine facts; provided declaration regarding business practices and lack of factual basis for claims. Source code at issue was written in a web-host scripting language.
	Status:	Settled

Date:	2006	**Gordon & Rees (for Defendants)**
	Case	Microsoft vs BWT Industry Technology
	Project:	Provided expert opinion regarding alleged pirating of Microsoft products.
	Status:	Settled

Date:	2006	**Greenan, Peffer (for Defendant & Cross-Complainant)**
	Case	Benedict v Mediatrac
	Project:	Expert testimony at a jury trial regarding standard level of care relating to IT practices.
	Status:	Jury award for Defendant
	Testimony:	Jury trial regarding software coding and management standards; deposition

Date:	2006	**Jones Day (for Plaintiff)**
	Case	ST vs SanDisk
	Project:	Patent infringement regarding semiconductor design techniques and ESD circuits. Investigation in support of claim construction and non-infringement analysis.
	Status:	Settled
Date:	2007	**McDermott Will & Emery (for Plaintiff)**
	Case	Matsushita v. MediaTek
	Project:	Patent infringement investigations (validity, claim construction, infringement) relating to various patents, including phase-lock loop design.
	Status:	Settled
Date:	2006	**Dechert LLP (for Plaintiff)**
	Case	Silvaco vs BindKey, et al
	Project:	Analysis and declarations regarding misappropriation of Silvaco trade secrets, including forensic analysis of hard disk drives used by defendants. The source code was written in C++.
	Status:	Settled
Date	2007	**Buchanan Ingersol (for Plaintiff)**
	Case	Shore Venture Group v Authentidate
	Project:	Analysis of source code relating to misappropriation of trade secrets and literal copying of source code.
	Status:	Completed
Date	2007	**American Assoc of Arbitration**
	Case	Panpacifics v Tradebeam
	Project	Selected as an independent expert to assist the arbitration panel with technology issues
	Status:	Settled
Date	2007	**Millberg Weiss (for Plaintiff)**
	Case	Shareholders v Magma
	Project	Documented facts relating to the technical aspects of false and misleading statements made by Magma. Provided technical consulting service to plaintiffs counsel to explain the scope and nature of the Defendants acts.
	Status	Setttled
	Expert Report:	Addressed industry-standard software coding practices and level of care relating to possible misappropriation of trade secrets by employees, misappropriation of trade secrets

Date	2007-	**Miller Barondess (for Plaintiff and Cross-defendant BHE)**
	Case	BHE Group v MTS Products
	Project	Analysis of expert testimony; investigation relating to performance of computers
	Status	Won jury award in excess of $45,000,000 for client, BHE
	Testimony	Testified at jury trial relating to adequacy of the design of laptop computers; deposition.
Date	2007-	**Synopsys, Inc.**
	Projects:	IP-related consulting activities regarding patents and patent strategy
	Status:	Ongoing
Date	2007-08	**Dechert, LLP (for cross-complainant Acer, Inc)**
	Case	HP v Acer
	Project	Retained as testifying expert. Analyzed ICs regarding infringement of Acer's circuit design patents. Analyzed and documented infringement of several different ICs. Research included on-site inspections of IC designs using owner-supplied design tools to demonstrate infringement.
	Status	Settled
Date	2008	**Bergeson, LLP (for defendant Clarus)**
	Case	Variphy, Inc. et al, v Clarus Systems, Inc.
	Project	Investigate alleged misappropriation of trade secrets and source code copying of VoIP telephony and related applications.
	Status	Settled
Date	2008	**Wilson Sonsini (for plaintiff Sandisk Corporation)**
	Case	Sandisk v various Flash memory manufacturers
	Project	Retained as consulting expert responsible for analyzing flash memory controller products for possible infringement of SanDisk patents. Analyzed the detailed design of various products and prepared infringement analyses. Support depositions of technical personnel and experts.
	Status	Complete
Date	2008	**Wilson Sonsini (for defendant Go Daddy)**
	Case	Web.com v Go Daddy
	Project	Prepared and presented claim construction tutorial explaining the background technology for 4 web-hosting related patents
	Status	Settled
	Testimony:	Markman tutorial explaining technology for the web-hosting patents at issue.

Date	2007-	**Jones Day (for Plaintiff On Semi)**
	Case	On Semiconductor v Samsung
	Project	Retained as testifying expert. Performed research to determine infringement and validity of four patents. Three of the patents related to circuits; one related to metallization systems. Prepared expert reports regarding infringement and validity. Prepared declarations in support of various discovery motions. Prepared Markman tutorial for all patents at issue. Assisted attorneys in deposition of Samsung's expert and other technology witnesses.
	Status	Settled
	Testimony	Deposition
	Expert Reports:	Relating to validity and infringement of three circuit-related patents and one metallization process technology patent

Date	2008-	**Wilson Sonsini (for defendant Synopsys)**
	Case	Ricoh v Synopsys
	Project	Consulting expert. Prepared technology tutorial. Researched and assisted in preparation of a Motion for Summary Judgment for non-infringement and reply.
	Status:	Ongoing

Date	2009	**King and Spalding (for Plaintiff Spansion)**
	Case	Spansion v Samsung (ITC and District Court actions)
	Project	Consulting expert. Provide analysis and discovery advice on evidence needed to demonstrate infringement of the patents at issue.
	Status	Ongoing

Employment History

From:	2001	**Brass Rat Group, Inc.**
To:	Current	Woodside, CA
	Position:	*CEO*
		Brass Rat Group is a successful Silicon Valley based consulting organization specializing in litigation consulting and business consulting in the semiconductor (IC) design field. Dr. Walker provided litigation support and expert analysis for plaintiff Synopsys in Synopsys vs Nassda, which was recently settled resulting in a "significant victory" for Synopsys.

From:	2000	**Knowledge Networks**
To:	2001	Menlo Park, CA
	Position:	*Chief Technology Officer*
		Knowledge Networks is a pre-IPO market research company that is leveraging internet technology to revolutionize the market research industry. KN recruited a panel of over 50,000 consumers to be interviewed on a variety of topics weekly. Dr. Walker managed KN's

engineering group, which designed and created automated systems to create surveys, conduct interviews, process data, and manage the panel. He also managed the IT group which was responsible for high-availability web-based systems for fielding the interviews as well as the internal systems required to analyze the data and produce real-time reports.

From: 1995
To: 2000
Position:

Sequence Design (Formerly Frequency Technology)

Founder, Founding CEO, Director & CTO

Sequence Design, formerly Frequency Technology, is the leader in the EDA segment called Design Closure. Sequence's products and services, consisting of pre- and post-layout optimization based on accurate layout extraction, enable designers to bring higher performance, lower-power integrated circuits quickly to tape out. Dr. Walker:

- Developed business plan and raised over $9MM in financing;
- Hired staff and led development, including defining technical product definition; Personally developed many of the basic algorithms, which resulted in five issued patents;
- Led initial marketing efforts;
- Wrote numerous technical articles advancing the company's technical position;
- Served as chief technical spokesman for the company.

From: 1990
To: 1995
Position:

Symmetry Design Systems
Los Altos, CA

Founder, Director & Executive Vice President

Symmetry, a self-funding enterprise, was a service and product business specializing in the analog simulation EDA market. Products included simulation-model libraries, modeling tools, and special-purpose analog simulators. Dr Walker was responsible for a joint venture in Beijing China, where new products were developed. Symmetry was acquired by Analogy, Inc.

- Initiated Japanese and European marketing activities.
- Developed conceptual framework and user-interface model for the Sun OpenLook-based product.
- Served as technical spokesman in customer and industry forums.
- Conducted sales training in the US, Asia, and Europe.

From: 1983
To: 1990
Position:

Analog Design Tools
Sunnyvale, CA

Founder, Director, Founding CEO & Chief Scientist

ADT's first product, the Analog WorkBench, pioneered the market for Analog CAE workstations, including such fundamental concepts as multiple window CAE systems, and simulated test instruments as a paradigm for CAE user interface. ADT, which had grown to $16MM in

annual sales and 150 employees, was acquired by Cadence.

- Formulated original business plan and presented concept to venture investors. Raised initial venture financing. Led fund-raising activities through the series C round.

- Served as President during formative stage. Director and Chief Scientist (CTO) from the founding through acquisition. Set the product direction. Drove the technology development.
- Formulated ADT's initial marketing strategy. The international distribution strategy focused primarily on Japan.
- Developed the Japanese market for ADT's products. Responsible for establishing and maintaining our distributor relationship, negotiating contracts, supporting customers, and building sales that amounted to 20% of the installed base.

From: 1980 **COMSAT**
To: 1983 Palo Alto, CA
Position: *Director, Microwave Systems*
Managed a Navy sponsored program to develop high productivity techniques for manufacturing of microwave components. Developed a microwave circuit-synthesis product.

From: 1973 **Watkins-Johnson**
To: 1980 Palo Alto, CA
Position: *Member of the Technical Staff*
Developed GaAsMESFET-based microwave amplifiers, components, and tuners. Designed and produced the world's first GaAsMESFET amplifiers to be delivered in production quantities.

Consulting History (within last 5 years)

From: 2005 **Sequence Design**
To: 2007 Santa Clara
Duties: EDA software analysis

From: 2005 **Sabio Labs**
To: 2006 Palo Alto, CA
Duties: Created business plan, operating plan, and marketing plan for EDA startup focused on analog circuit optimization and synthesis

From: 2005 **Synopsys, Inc**
To: On-going Mountain View, CA
Duties: Technology investigations relating to IP issues. Presented technology overview to non-technical staff

Martin G. Walker, PhD
Consultant Curriculum Vitae

Patents

Patent Number	Date Issued	Title
6,643,831	2003	Method and system for extraction of parasitic interconnect impedance including inductance
6,381,730	2002	Method and system for extraction of parasitic interconnect impedance including inductance
5,901,063	1999	System and method for extracting parasitic impedance from an integrated circuit layout

Education

Year	College/University	Degree
1987	AEA/Stanford Executive Institute	Completed w/distinction
1979	Stanford University, Stanford, CA	Ph.D., Electrical Engineering
1976	Stanford University, Stanford, CA	MS, Electrical Engineering
1973	Massachusetts Institute of Technology, Boston, MA	BS, Electrical Engineering

Publications

Over fifty articles in the fields circuit design and design automation, including technical papers in peer-reviewed journals, an invited article in the IEEE Spectrum, and various conference proceedings. I have organized seminars, which were designed to enhance the technical credibility of my companies, and written numerous opinion pieces published in journals such as EETimes that served to establish and promote our corporate position. Some more recent publications are listed below.

Martin G. Walker, Modeling the Wiring of Deep Submicron ICs, IEEE Spectrum Vol 37, No. 3, March 01, 2000 at pp. 65-71.

Martin G. Walker, Keh-Jeng (KJ) Chang, Christopher J. Bianchi, SIPP's Why Do We Need a New Standard for Interconnect Process Parameters? VLSI: Systems on a Chip, Kluwer Academic Publishers, December, 1999.

Martin Walker, Timing Errors Haunt Interconnects, Electronic Engineering Times No. 1021, August 17, 1998.

Martin Walker, Interconnect Analysis Must Move to 3-D, Electronic Engineering Times No. 980, November 10, 1997.

Martin G. Walker, The Guardband Crisis, Electronic Engineering Times No. 929 November 25, 1996 at p. 43.

In addition to the foregoing, I also submitted opinion pieces to Integrated Systems Design (May 1997), Electronic Business (April 1998), and EE Times (June, July, and September 1998).

Professional Associations and Achievements

- 1999 Fortune Magazine "Cool Company" for Frequency Technology.
- 1984 Electronic Products New Product of the Year award for the Analog Workbench
- 1976 IEEE Microwave Applications award recognizing contributions to the design of GaAsFET amplifiers.